EE/CprE/SE 492 WEEKLY REPORT 02

9/1/2020 – 9/14/2020

Group number: 08

Project title: High Resolution Digitally Trimmable Resistor

Client &/Advisor: Prof. Randy Geiger

Team Members/Role: Clark Reimers - Test Engineer, Pierce Nablo - Design Engineer, Alek Benson - Information Manager, Oluwatosin Oyenekan - Meeting Lead

❖ Weekly Summary

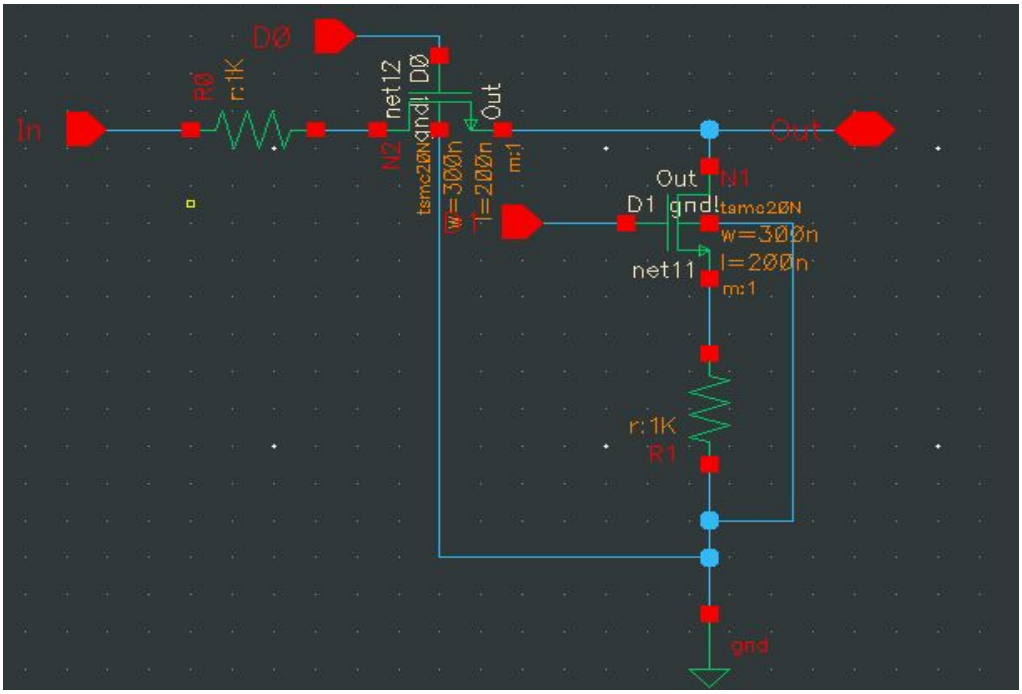
During the past 2 weeks our group has been working on simulating a few different circuit structures. One of them was the nested ladder structure, one was a voltage divider type resistor, and then a larger version of the ladder. We looked at the effects of the TCR when we had different bit combinations active for the circuits. Also we did the PIRM presentation to show our other classmates what we have been up to.

❖ Past week accomplishments

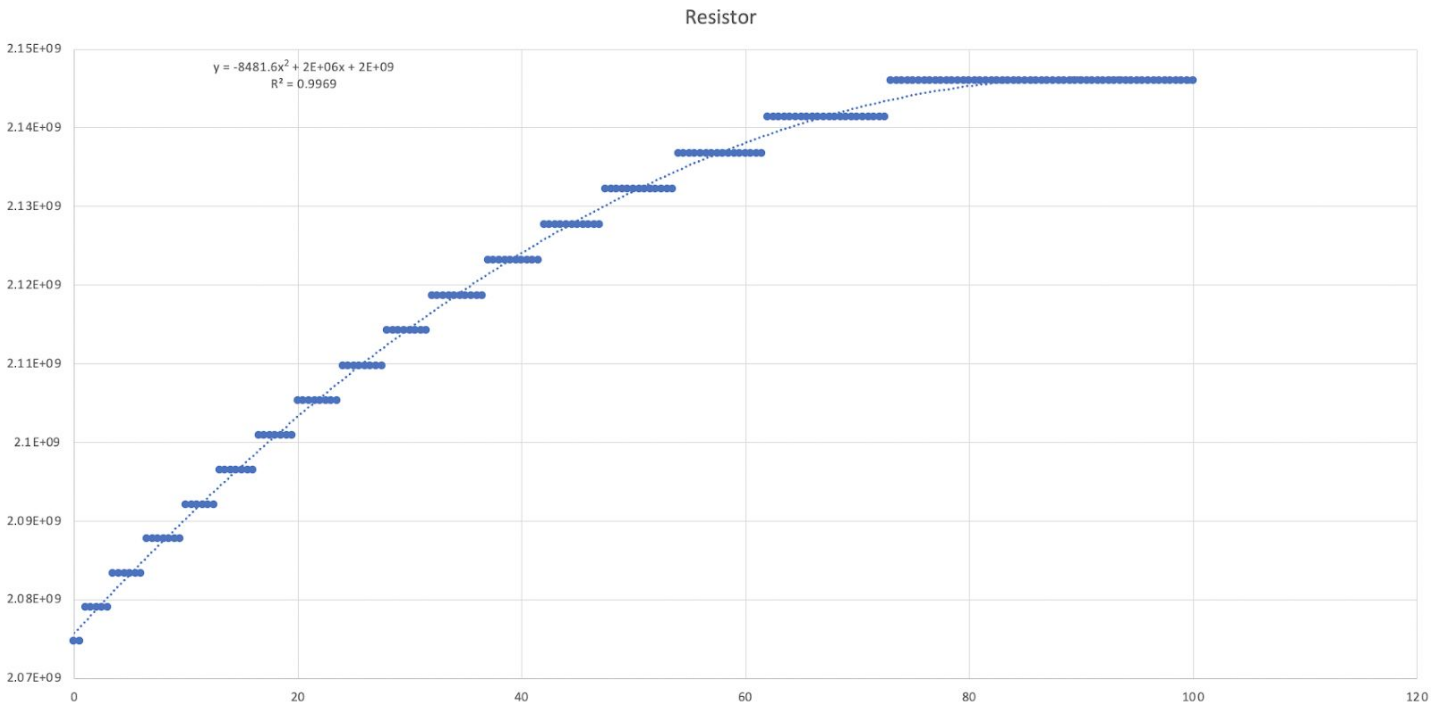
Clark Reimers:

- Continued working with the voltage divider structure
    - Attempted to find TCR.
    - Debugging testbench.
- Started working on identifying some other structures for test
- PIRM presentation

Voltage divider structure



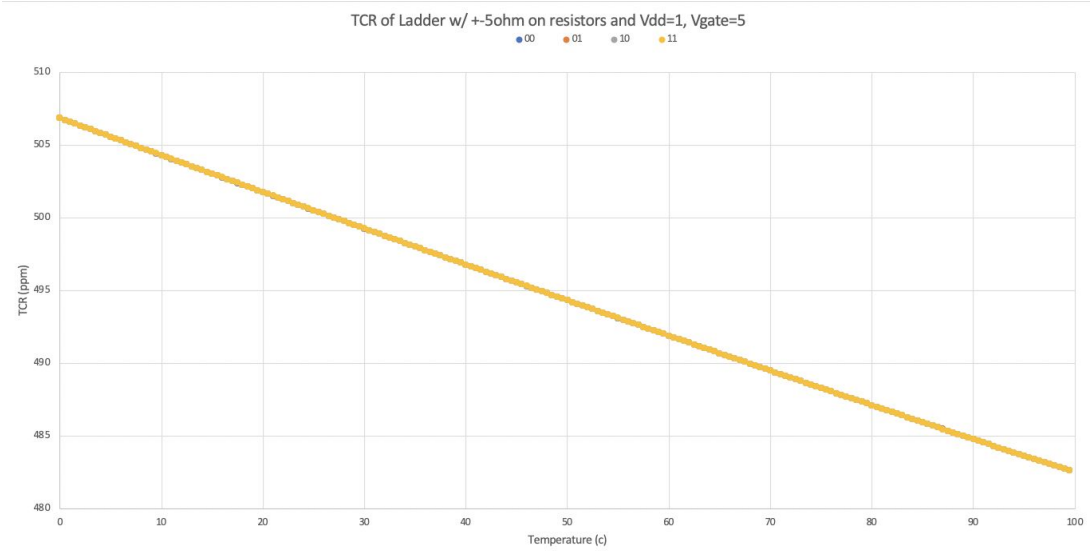
TCR:



Pierce Nablo:

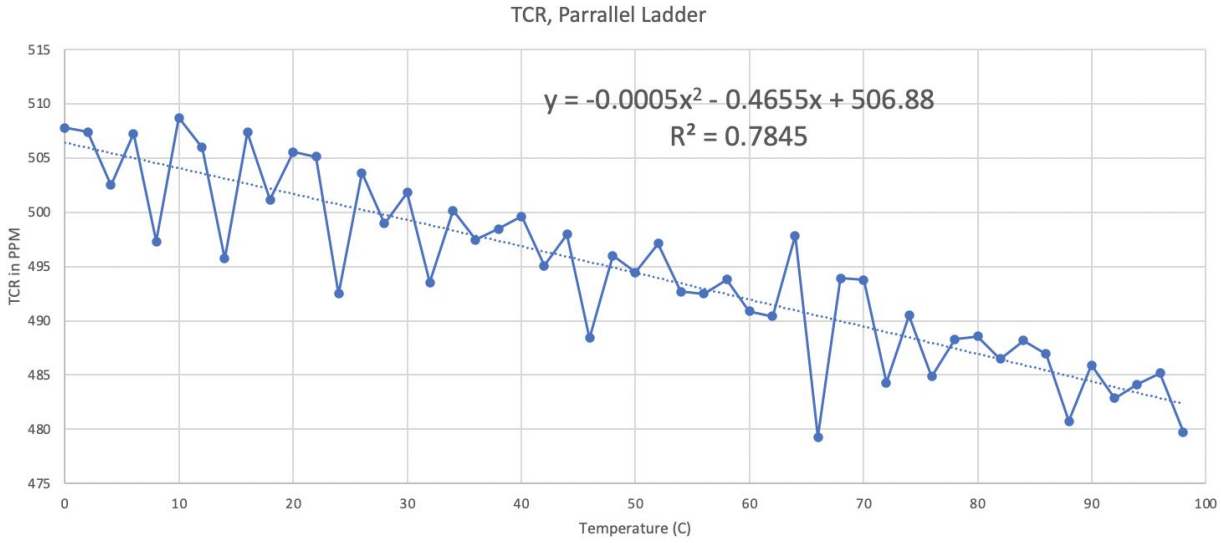
- Fixed my simulation errors which were from forgetting to include a ground in the circuit
- Fixed an error that was causing the TCR calculations to be wrong. I was not subtracting Vdd from the voltage at the output node.
- Tested the ladder structure again but this time I was changing the bit combinations to see if that would have any effect on the TCR. Then plotted the results in excel.
- Participated in the PIRM presentation for the senior design class

Ladder 2 Bit structure



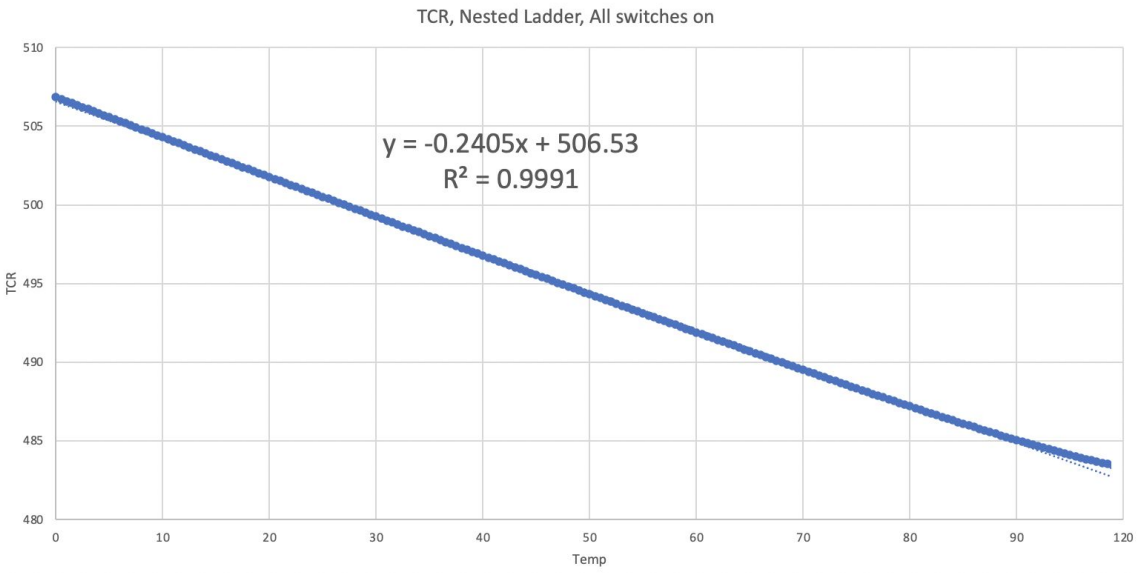
The chart above shows the plots for the 4 different bit combinations. All the plots are on top of one another.

Ladder 2 Bit, subassembly wired in parallel



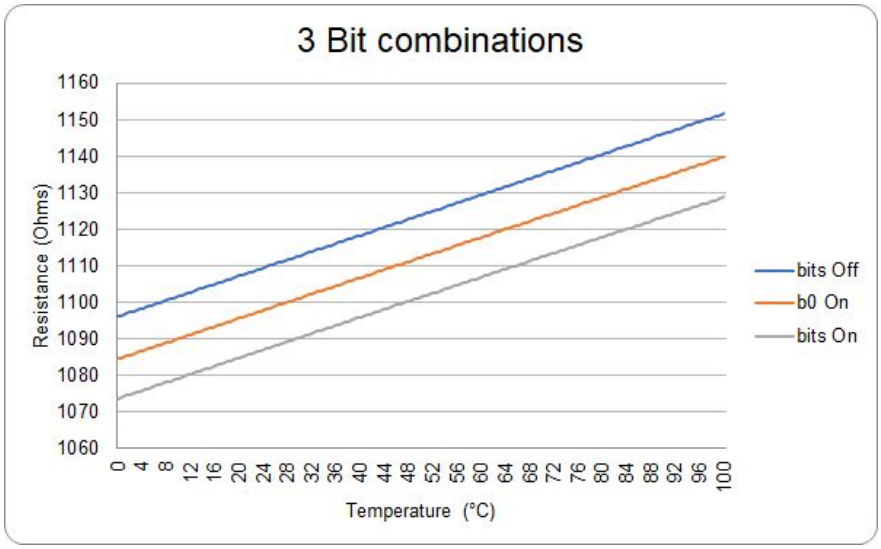
The chart above shows the TCR of the parallel circuit structure.

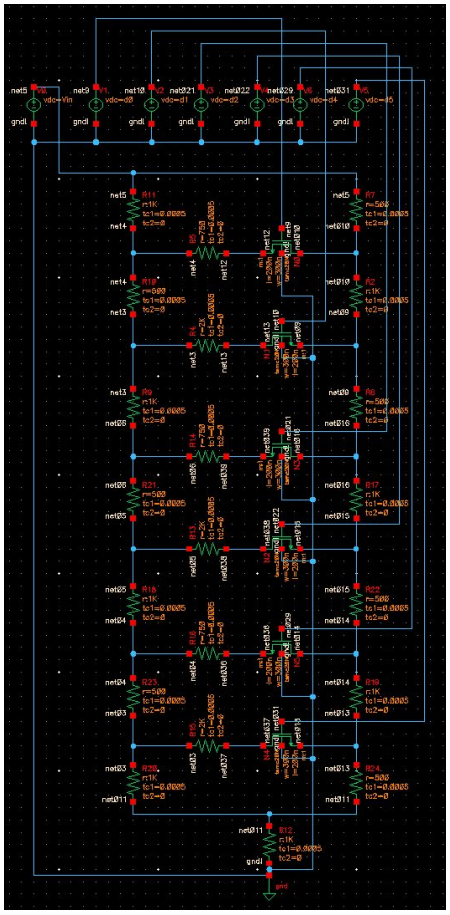
Ladder 2 Bit nested structure



Fixed the TCR plot for the figure shown above.

Alek Benson:

- Revised some simulation parameters in spectre.
- Found equivalent resistance for 2 bit ladder structure.
- Mapped out resistance values for ladder structure.
- Achieved 1% resolution on 2 bit ladder structure.
- Simulated temperature coefficient of current ladder structure layout
- Documented findings in presentation and report.
- Scaled up basic version of ladder schematic
- Sent many emails trying to communicate scheduling conflicts
- 

- 

Oluwatosin Oyenekan:

- Did some research on how to find the temperature coefficient of a circuit and was confused until meeting with dr geiger who cleared it up.
- Researched how the ladder structure would be able to trim a resistor and tried to understand the math behind it
- Participated in the PIRM presentation for the senior design class

❖ **Pending issues**

Clark Reimers:

- No issues

Pierce Nablo:

- No issues

Alek Benson:

- No Issues

Oluwatosin Oyenekan:

- No Issues

❖ **Individual contributions**

Name	**Hours 8/30 - 9/5**	**Hours 9/6 - 9/13**	**Hours cumulative**
Clark Reimers	8	7	31
Pierce Nablo	7	7	32
Alek Benson	7	9	32
Oluwatosin Oyenekan	7	8	30

- **Plans for the upcoming week**

  Clark Reimers: I want to continue working on coming up with some new designs to simulate and compare to our reference designs. The plan will be to find a structure with resistor TCRs that are equal to each other and expand on that. I also need to continue debugging the voltage divider structure.

  Alek Benson: The plan for the upcoming week is to first come to an understanding with Dr. Geiger and the group about a temperature range to find the TCR. Also, I will continue to modify the ladder structure to do some larger scale trims. Another goal is to simulate the re-configured ladder structure in order to get TCR data, and compare it to other schematics. Lastly the series structure will be re-configured to modify trim resolution and transistor sizes.

  Oluwatosin Oyenekan: The plan for this week is to take up on Dr Geiger explanation on the ratio for the tcr and use it to figure out the TCR for the circuit designs and the reference circuit and compare them together.

  Pierce Nablo: Look at the circuit Clark was making based on the voltage divider structure and see if I can get that to generate something realistic.

- **Summary of weekly advisor meeting**

  We were able to meet at the end of the second week of this reporting period. It took a while to finally establish communication with Dr. Geiger, but we have successfully planned a recurring meeting schedule for the rest of the semester. The week before we were not able to meet and spent time trying to communicate with one another and Dr. Geiger, as well as other project related work. During the meeting on Friday, we presented a slideshow that we put together to clearly discuss our progress and plans. We showed Dr. Geiger some of our errors in simulations we were encountering, some results from other simulations, future schematic ideas, and methods for comparison of the different schematics. Overall, we made good progress during this meeting, and have a good idea of how to continue to progress on the project.